ABSTRACT

An address translation mechanism is provided for use in a partitionable server. In one embodiment, the address translation mechanism provides a sequential zero-based physical memory address space to each of the server's partitions. The translation mechanism maintains mappings between the partitions' physical memory address spaces and a machine memory address space that maps to the real (hardware) memory of the server. The translation mechanism transparently translates physical addresses referenced in memory access requests into machine addresses. As a result, conventional operating systems and other processes that are designed to access sequential zero-based addressed spaces may execute in partitions of a partitionable server without modification. Techniques are also provided for remapping a range of physical memory addresses from one machine (hardware) memory resource to another in a partitionable server, thereby enabling machine memory to be replaced without requiring the server to be rebooted.